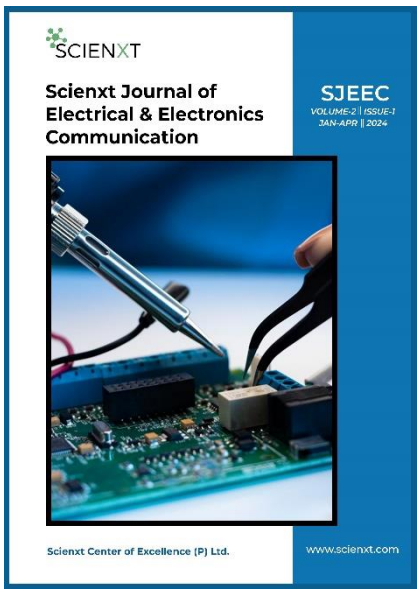

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A review on low power circuit technique for improved feed through logic

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Abstract:

This review paper examines the advancements, challenges, and applications of low power circuit techniques utilizing improved feed-through logic. With the increasing demand for energy-efficient electronic devices, feed-through logic presents a promising alternative to traditional CMOS logic by leveraging the inherent capacitance of transistor gates to minimize power consumption while maintaining performance. The abstract explores the fundamental principles of feed-through logic, its advantages over conventional logic families, and the methodologies employed in its design and optimization. Additionally, the abstract discusses application scenarios across various domains, including IoT devices, wearable electronics, medical implants, and aerospace systems. Case studies demonstrating the power efficiency of feed-through logic in real-world applications are examined, highlighting its potential to extend battery life and enhance reliability. Finally, practical implementation considerations such as technology compatibility, design tools, reliability, and system integration are discussed. Through a comprehensive review of the literature, this abstract provides insights into the capabilities and future prospects of low power circuit techniques based on improved feed-through logic.

Keywords:

FTL, Dynamics CMOS Logic Circuit, Low Power Adder, DVFS