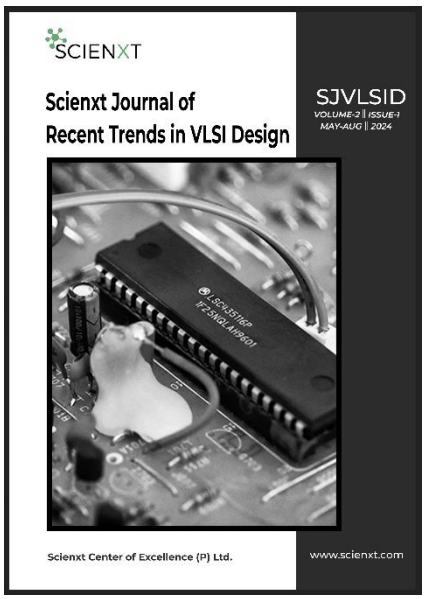

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Highly efficient 4:2 compressor using carry based approximate full adder on digital circuit design

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Abstract:

The 4:2 compressors have been widely used in multiplier realizations. For rapid digital arithmetic integrated circuits, we suggest a very efficient 4:2 compressor circuit. Four: 2 compressor circuits were built using a carry-based approximation full adder. In error-tolerant applications where precise processing units are not always essential, approximate computing can decrease design complexity while enhancing performance and power efficiency. They can be substituted with their approximate counterparts. A new design technique for carrying-based approximation of full adders has been modified to include variable probability terms. Most multimedia programs can glean useful information from slightly erroneous results. As a result, we do not need to generate precise results. This short introduces a novel gate level logic modification technique for approximating a full adder in order to take advantage of the relaxation of numerical exactness. For reducing the area, the sum term is changing to recommend the carry-based approximation adder (CBAA) instead of the considerable XOR operation in the typical full adder. The power consumption, area, and delay of the suggested 4:2 compressor circuit were compared to previously reported circuits, and the proposed circuit was found to have the lowest power consumption, least area, and least delay. It is recommended to employ a Proposed Compressor to increase efficiency while decreasing error rate. VHDL circuit construction is simulated by using Xilinx ISE 14.7.

Keywords:

Approximate computing, Carry based approximate adder, Area efficient, 4:2 Compressor, VHDL