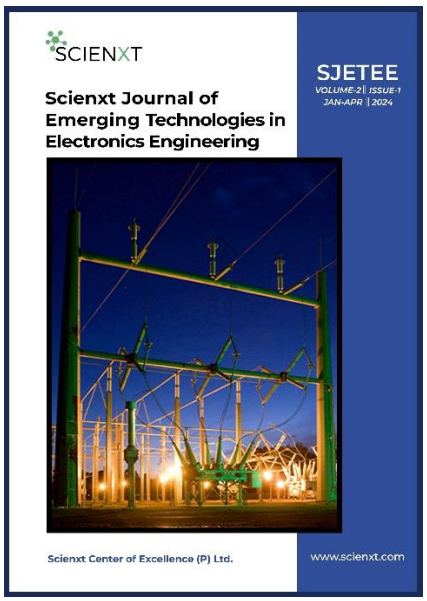

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A 24-32 GHz single-chip harmonic balance power amplifier for 5G MW application

[*1]Dr. Pritesh Tiwari, [2]Puja, [3]Ekta

[*1](Associate Professor) Department of Electronics & Communication Engineering Bhopal institute of technology and science,Bhopal

[2] (Student) Department of Electronics &Communication Engineering Bhopal institute of technology and science,Bhopal

[3](Student) Department of Electronics &Communication Engineering Bhopal institute of technology and science,Bhopal

**Corresponding Author:*
Email:

Abstract:

This article introduces the CM output-matching networks in the Balance architecture and discusses the theory and design process of a broadband RF-input Class-F PA balanced power amplifier. The harmonic balance network ensures the operation of second and third-harmonic and determines output impedance for wideband response. The input MN is considered as a band-pass filter. The reactance is taken from IMN. It stabilized the operation the design. The suggested HBPA's results show an output power of up to 30.9 dBm, more peak power-added efficiency (PAE) of 35.6% at 27 GHz, and a small signal gain of less than 28.6 dB. Over the 24–30 GHz range, saturated output power (Psat) and uniform gain are both reached with variations of less than 0.8 dB.

Keywords:

Harmonic Balance Power Amplifier, GaN HEMT, LDMOS, power-added efficiency (PAE)