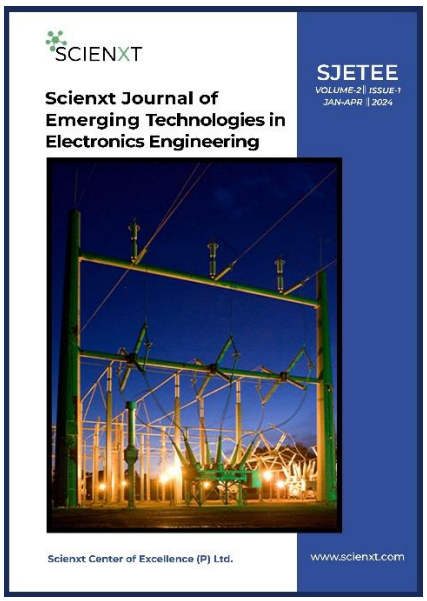

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A 24-32 GHz single-chip harmonic balance power amplifier for 5G MW application

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Abstract:

This article introduces the CM output-matching networks in the Balance architecture and discusses the theory and design process of a broadband RF-input Class-F PA balanced power amplifier. The harmonic balance network ensures the operation of second and third-harmonic and determines output impedance for wideband response. The input MN is considered as a band-pass filter. The reactance is taken from IMN. It stabilized the operation the design. The suggested HBPA's results show an output power of up to 30.9 dBm, more peak power-added efficiency (PAE) of 35.6% at 27 GHz, and a small signal gain of less than 28.6 dB. Over the 24–30 GHz range, saturated output power (Psat) and uniform gain are both reached with variations of less than 0.8 dB.

Keywords:

Harmonic Balance Power Amplifier, GaN HEMT, LDMOS, power-added efficiency (PAE)

1. Introduction:

A power amplifier (PA) is the most power-hungry component in the front end of the system, its efficiency is crucial to the operation of a 5G transmitter. Additionally, in 5G applications, for small cells, the need for a compact PA design becomes essential. The bandwidth is another crucial design factor to consider (BW). The transmitter design can be made simpler by accommodating more wireless communication standards with a higher BW of the PA. [1]-[2]. There are several benefits and difficulties associated with introducing a practical harmonic balancing capability at the device measurement stage. To overcome this conventional barrier, the test-bench engineer must learn more about the requirements and design process [3]. It is not always possible to achieve high efficiency with flawless harmonic processing, such as class F. Using the authors' non-linear transistor model, harmonic balance analysis was used to determine the ideal harmonic reflection phases [4]. A high-power level with high even-order suppression is demonstrated in the broadband power amplifier [5]. An LDMOS device with high power, bias circuitry, and a matching network in a simulation of harmonic balance is discussed [6]. First, investigated how the load variation caused by the second and third harmonics affected the level of power-added efficiency (PAE). To achieve the necessary PAE level and high gain values, the optimal third harmonic load values are selected, which form the basis of the proposed design [7]. The effect of load variation on the second and third harmonics on the power-added efficiency (PAE) [8]. An exact large-signal model that was extracted for the GaN devices serves as the foundation for both harmonic tuning and load modulation.[9]. To enable self-consistent device simulation using full-band Monte Carlo particle-based simulation, a Harmonic Balance (HB) frequency domain circuit solver was created. [10]. A low pass filter (LPF) and a bias circuit (BC) make up the unique harmonic control network (HCN) that serves as the foundation for the design process [11]. Introducing the control amplifier's (CA) expanded range of second-harmonic load manipulation [12]. However, because of the somewhat complex output network with high-order harmonic terminations, there are problems with efficiency and chip size. Still exist. Furthermore, if the device parasitics—particularly the power transistor's large output capacitance—are not properly considered, they could significantly impair the PA's performance. This paper presents a class F MMIC power amplifier that uses 0.25 μm GaN HEMT technology to have both second and third harmonic terminations.

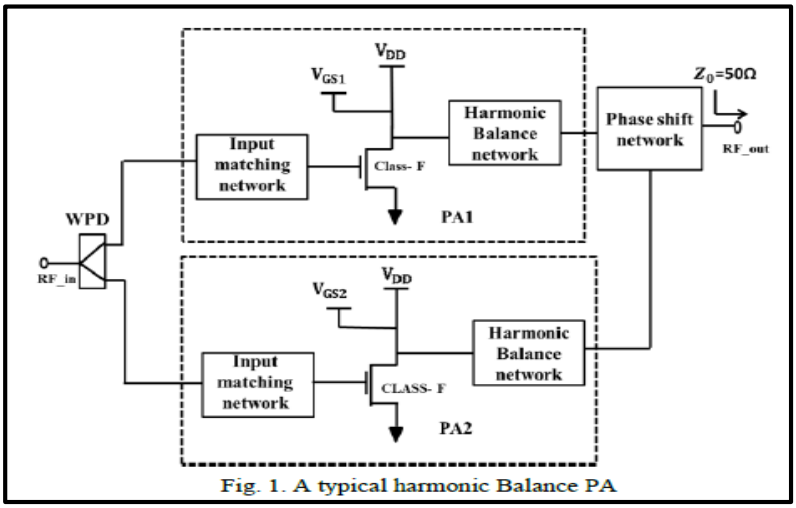

Figure. 1: A typical harmonic balance pa

Semiconductor focused on small cell applications for 5G. It is demonstrated to have a wide BW MMIC, high output power, and high efficiency. A Class-F balance PA is suggested in this paper for biomedical IoT applications. 5G MW.For 5G MW Applications, the suggested method provides a harmonic balancing network with increased bandwidth and a high gain. This paper's primary goal is to increase bandwidth and efficiency for 5G MW applications. The structure of the suggested work is as follows: Section II presents an overview of the design process. Overall results are shown in Section III, and Section IV presents the conclusions.

2. Circuit design and analysis:

This section covers the design of the proposed Harmonic Balance Power Amplifier based on Class-F PA. First, the Harmonic Balance Network is covered in subsection Asubsection B examines Second-Harmonic and third-harmonic manipulation; subsection C examines; Behavior Analysis, and subsection D reports on the final circuit.

2.1. Harmonic Balance Network:

As shown in Fig. 2, it should be measured at high power in a harmonic balance network. Parasite, um die Parameter Cout und Lout festzulegen. It is a star trap from harmonic tuning and imperfect transmission. Furthermore, it provides impedance matching at the fundamental frequency between the 50Ω load impedance and f0 input impedance of the operational frequency. The nonuniform transmission harmonic balance network with equal parts for the operation of open circuits. An open circuit between ideal impedance and fundamental impedance is provided by the capacitive network. Similarly, the nonuniform transmission line's third harmonic impedance is shorted. Demonstrates the fundamental-frequency impedance

matching at 24 GHz and the corresponding second and third harmonic tuning at 24 GHz and 32 GHz, respectively,

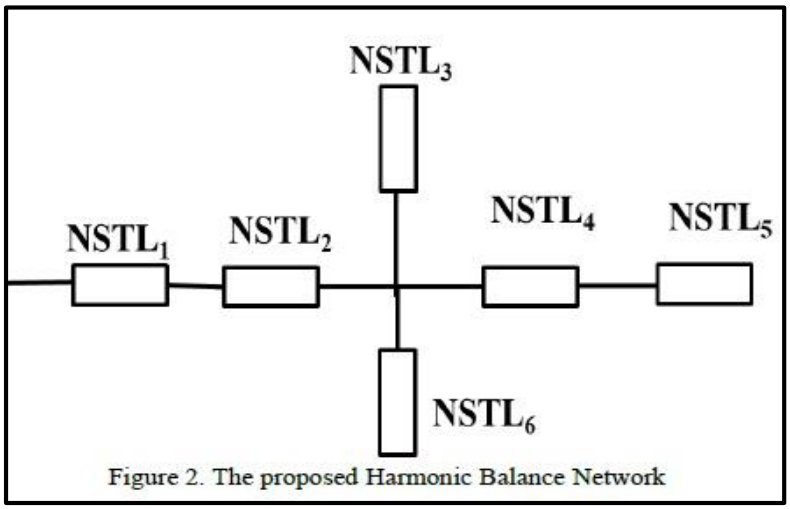

Figure. 2: The proposed harmonic balance network

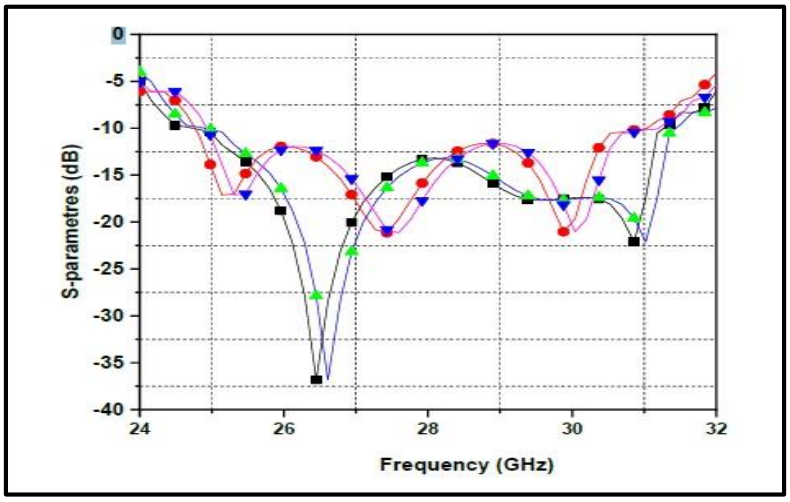

Figure. 3: Class F load network with second and third harmonic tuning and its frequency

2.2. Broadband Phase Shifter:

The proposed broadband phase shifter has five stubs short-circuit and five open circuits are inserted into the non-transmission line.to create a phase shifter for broadband. In a conventional transmission line, the phase variation is proportional to the operating frequency and can be compensated for by the open-circuit and short-circuit stubs. Over a broad frequency range, the resulting phase variations of the stubs and the transmission lines can be made to be nearly identical. Determine the characteristic impedance of the stubs to obtain flat relative phase differences between two sections. The full-wave scattering parameters are simulated using the commercial program ADS, based on the previously stated physical dimensions. Figure 3 shows the simulated frequency responses of the suggested hybrid coupler. Regarding the figure, the fractional bandwidth is 82% and the bandwidth for the port reflection coefficients ranging from

1.84 GHz to 4.3 GHz is observed at no more than –15dB. Consequently, there is good impedance matching between the input and output ports.

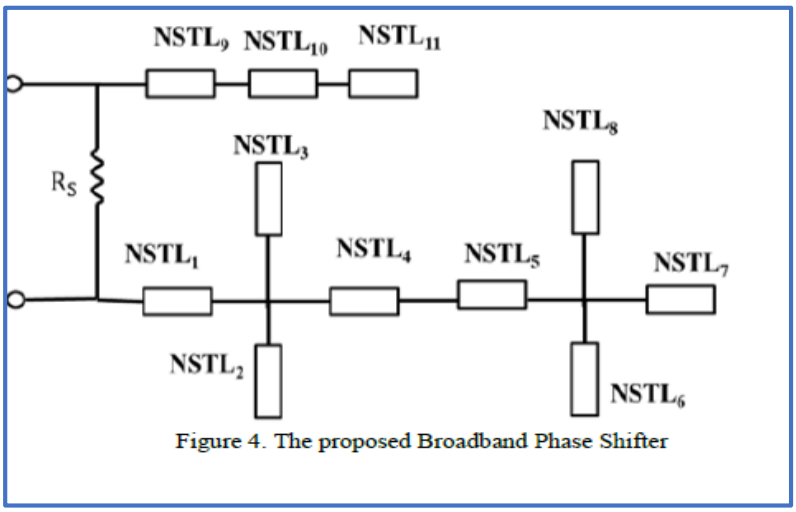

Figure. 4: The proposed broadband phase shifter

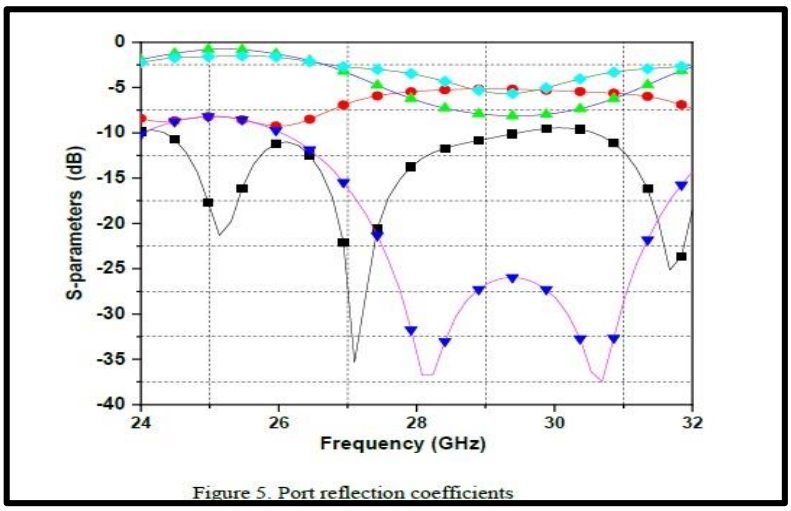

Figure. 5: Port reflection coefficients

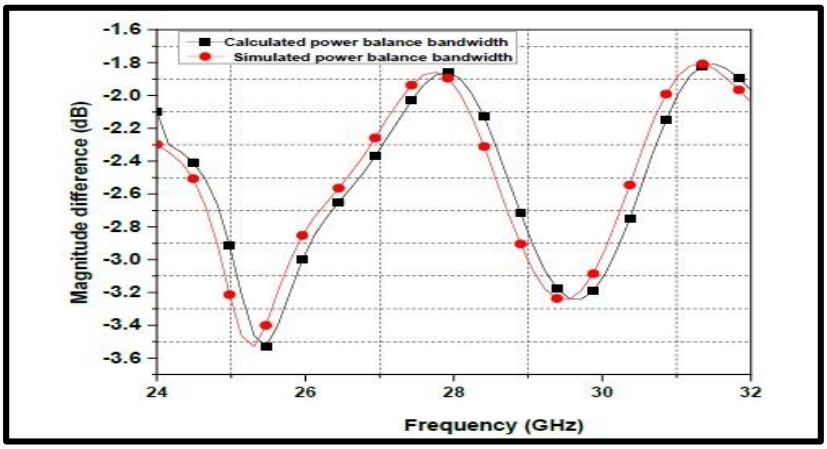

Figure. 6: Port isolation of the proposed Phase Shifter

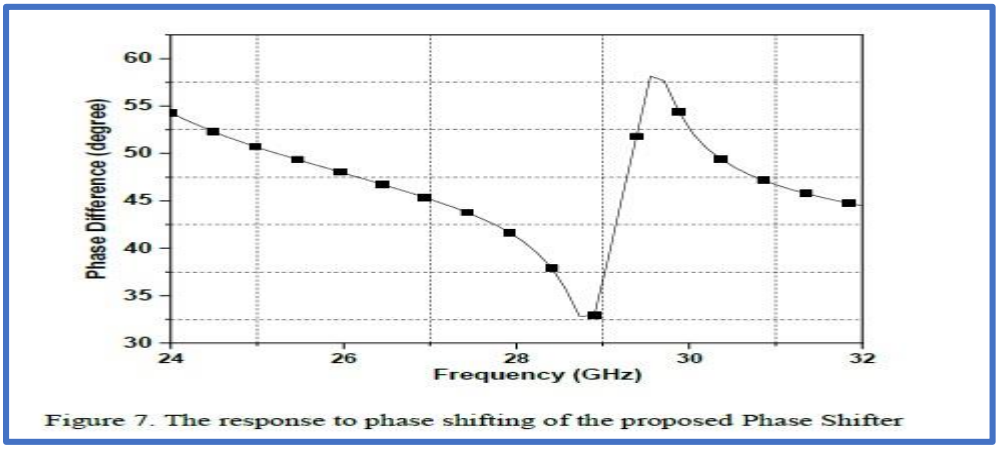

Figure 7. The response to phase shifting of the proposed Phase Shifter

2.3.Balance PA With Harmonic Network:

Using ADS modeling, the Doherty response of the balanced amplifier is confirmed over the intended bandwidth of 24-32 GHz, based on the proposed Harmonic balance and broadband PAs. In the first evaluation, which accurately depicts the suggested circuitry depicted in Fig. 6, the isolation port of the output coupler is shorted to RF ground using a cin= 100-pF capacitor. The figure illustrates how this PA's intended Doherty behavior can be attained at several frequency points over the design frequency range. When the peaking amplifier shuts off, the landing points of this set of trajectories are in the intended high impedance zone, which supports the active load modulation of the HB PA nicely.

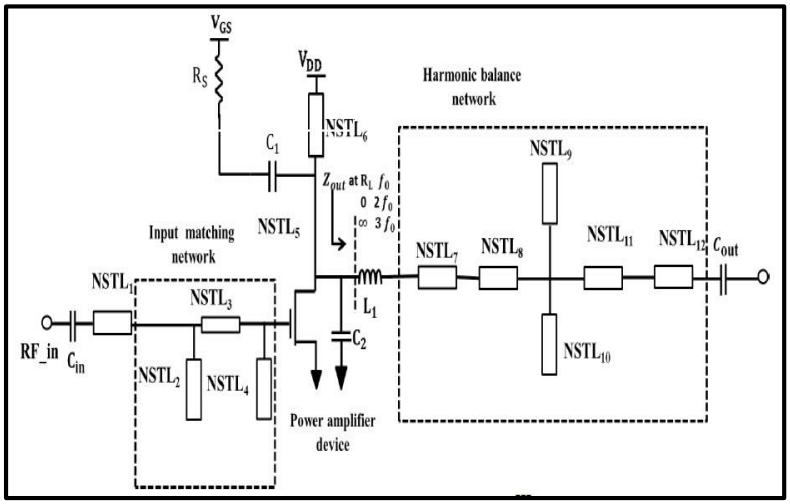

Figure. 8: Proposed circuitry of Harmonic Balance Power Amplifier

3. Results and discussion:

Fig. 9,10,11 reports single-tone characterization results compared to simulations. For the Tuned Load and Harmonic Tuned PAs, respectively, the saturated output power is 35.6 dBm and 36.6

dBm, with matching efficiencies of 68.5% and 59%, and a little signal gain of 10.7 dB and 12 dB.

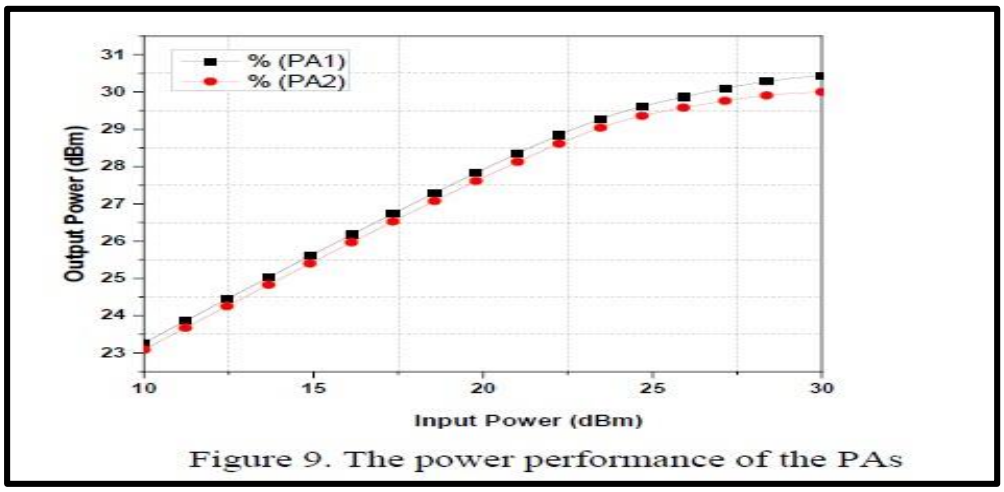

Figure. 9: The power performance of the PAs

Table. 1 shows a comparison of the frequency, saturated output power, and saturated efficiency of certain commercial GaAs PAs with the planned 24-32 GHz PAs. Performance is calculated in terms of efficiency and output power.

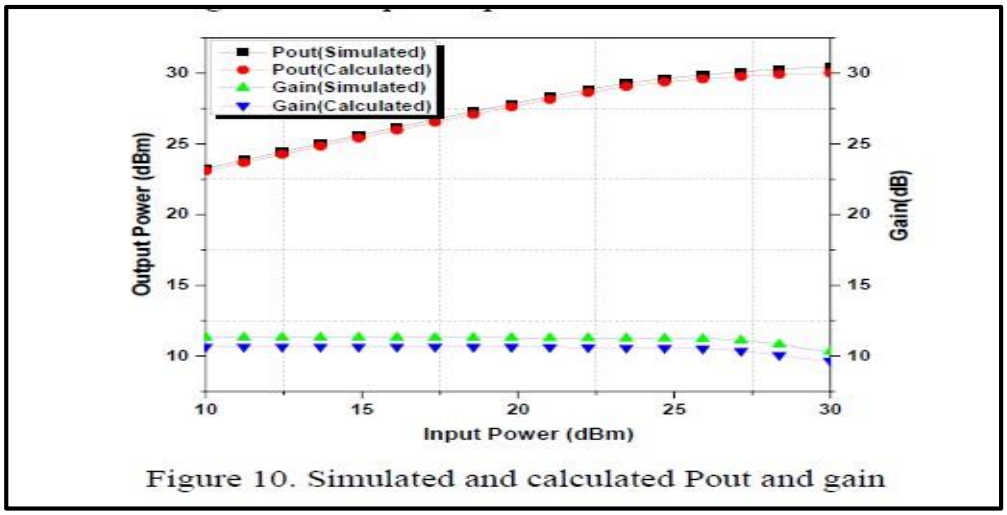

Figure. 10: Simulated and calculated pout and gain

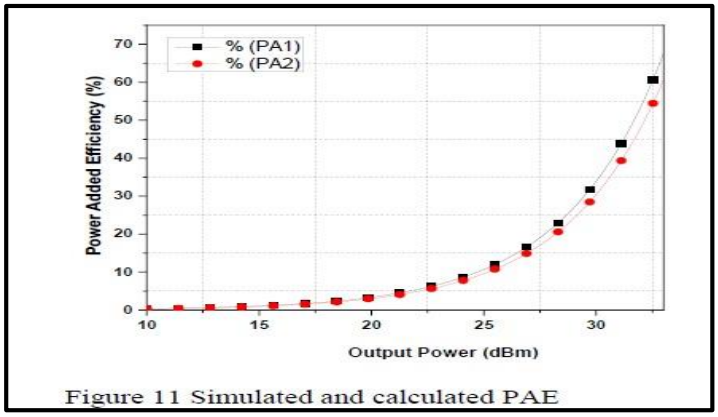

Figure. 11: Simulated and calculated PAE

Table. 1: Shows a comparison of Pas

References	*F (GHz)*	*Pout (dBm)*	*PAE (%)*	*Gain (dB)*
[12]	2.05-3.65	45	50-66	10
[13]	7.5-11.5	40	38	36.3
This work	24-32	34	67	12

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4. Conclusion:

A 1-watt GaN MMIC PA that is fully integrated and operates in the 24-32 GHz band is showcased. In this research. Important design factors are covered, including efficiency concerns, the best way to extract impedance and cell selection. The resultant MN was created by network synthesis. The load-pull optimization ensures the broadband operation. The interstage matching network reduces the transistor's gain roll-off. The input matching network is used for maintain a wideband response.

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