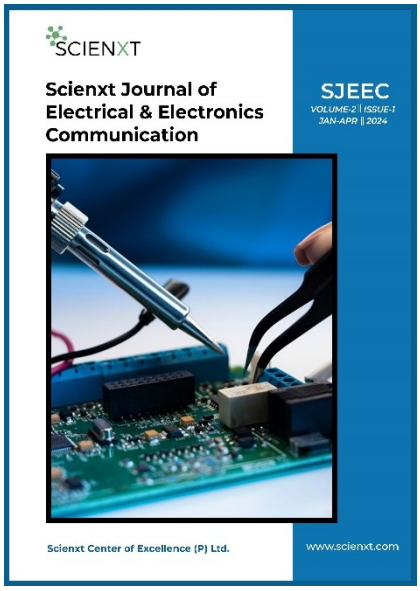

Scienxt Journal of Electrical & Electronics Communication
Volume-2 || Issue-1 || Jan-Apr || Year-2024 || pp. 1-14

A review on low power circuit technique for improved feed through logic

Prerna Wagadre[1], Niranjan Kumar[2], Md. Faizan[3], Ankit Kumar[4]

[1]Assistant Professor
[2,3&4]B.tech Scholars
Bhopal Institute of Technology, Bhopal 462045

**Corresponding Author: Prerna Wagadre*
Email: Prernawagadre@gmail.com

Abstract:

This review paper examines the advancements, challenges, and applications of low power circuit techniques utilizing improved feed-through logic. With the increasing demand for energy-efficient electronic devices, feed-through logic presents a promising alternative to traditional CMOS logic by leveraging the inherent capacitance of transistor gates to minimize power consumption while maintaining performance. The abstract explores the fundamental principles of feed-through logic, its advantages over conventional logic families, and the methodologies employed in its design and optimization. Additionally, the abstract discusses application scenarios across various domains, including IoT devices, wearable electronics, medical implants, and aerospace systems. Case studies demonstrating the power efficiency of feed-through logic in real-world applications are examined, highlighting its potential to extend battery life and enhance reliability. Finally, practical implementation considerations such as technology compatibility, design tools, reliability, and system integration are discussed. Through a comprehensive review of the literature, this abstract provides insights into the capabilities and future prospects of low power circuit techniques based on improved feed-through logic.

Keywords:

FTL, Dynamics CMOS Logic Circuit, Low Power Adder, DVFS

1. Introduction:

In recent years, the demand for low power consumption in electronic devices has surged dramatically, driven by the proliferation of portable devices, IoT applications, and energy-efficient computing paradigms. As a result, researchers and engineers alike have been compelled to explore innovative circuit design techniques to minimize power consumption while maintaining or even enhancing performance. Among these techniques, feed-through logic has emerged as a promising approach to achieve low power operation without sacrificing speed or area efficiency.

The relentless advancement of semiconductor technology has enabled the integration of billions of transistors onto a single chip, leading to unprecedented levels of computational power and functionality. However, this increased integration has also brought about challenges related to power consumption and heat dissipation. Traditional CMOS (Complementary Metal- Oxide-Semiconductor) logic, while highly efficient in terms of speed and reliability, tends to consume significant power, particularly in high-performance computing applications.

To address these challenges, researchers have been exploring alternative logic families and circuit architectures that prioritize energy efficiency without compromising on performance. One such approach is feed-through logic, which offers the potential for substantial power savings compared to conventional CMOS designs. By leveraging the inherent capacitance of the transistor gates, feed-through logic circuits can reduce switching activity and dynamic power dissipation, making them well-suited for low power applications [1-2].

Despite the promise of feed-through logic, its widespread adoption has been hindered by several challenges and limitations. Existing implementations may suffer from issues such as limited scalability, reduced noise margins, and increased design complexity. Furthermore, the performance trade-offs associated with feed-through logic must be carefully evaluated to ensure compatibility with diverse application requirements [3].

The need for comprehensive studies evaluating the efficacy of feed-through logic in various contexts and the development of optimized design methodologies is apparent. Additionally, there is a growing demand for systematic reviews that consolidate the existing body of research, identify key challenges, and propose avenues for future exploration.

In light of the aforementioned challenges and opportunities, this paper aims to provide a comprehensive review of low power circuit techniques leveraging improved feed-through

logic. The primary objectives of this review are as follows:

1) To examine the fundamental principles of feed-through logic and its advantages over traditional CMOS logic.
2) To survey the existing literature on feed-through logic design methodologies, optimization techniques, and implementation strategies.
3) To analyze the performance characteristics of feed-through logic circuits in terms of power consumption, speed, and area efficiency.
4) To identify the key challenges and limitations associated with feed-through logic and propose potential solutions.
5) To highlight emerging trends and future directions in low power circuit design leveraging feed-through logic.

By achieving these objectives, this paper aims to contribute to the ongoing discourse on low power circuit design and facilitate further advancements in the field.

This paper makes several contributions to the existing body of knowledge on low power circuit design and feed-through logic. Firstly, it provides a comprehensive overview of feed-through logic principles, design methodologies, and optimization techniques, thereby serving as a valuable resource for researchers and practitioners seeking to explore this promising approach. Additionally, through a critical analysis of existing literature and empirical studies, this paper identifies key challenges and opportunities for future research, paving the way for innovation in low power circuit design.

2. Literature review:

2.1. Overview of low power circuit design techniques:

Low power circuit design has become increasingly crucial in modern electronic systems due to the rising demand for energy-efficient devices across various applications such as mobile computing, IoT, and wearable technology. Several techniques have been developed to address power consumption while maintaining or enhancing performance. These techniques can be broadly categorized into architectural, algorithmic, and circuit-level approaches.

Architectural techniques focus on optimizing system-level parameters such as instruction set architecture, memory hierarchy, and data path organization to minimize power consumption

during operation. Examples include voltage scaling, clock gating, and power gating, which selectively disable or reduce the supply voltage to unused circuit blocks or modules.

Algorithmic techniques involve algorithm-level optimizations to reduce computational complexity and improve energy efficiency. These optimizations may include data compression, algorithmic approximation, and algorithmic transformations to exploit inherent parallelism and reduce power-hungry operations [2-4].

Circuit-level techniques, on the other hand, target power reduction at the transistor level by optimizing circuit topology, transistor sizing, and switching activity. Techniques such as threshold voltage scaling, multi-threshold CMOS (MTCMOS), and dynamic voltage and frequency scaling (DVFS) are commonly employed to reduce static and dynamic power dissipation in CMOS logic.

2.2. Introduction to feed through logic:

Feed-through logic is a promising alternative to conventional CMOS logic for low power circuit design. Unlike CMOS logic, which relies on the direct charging and discharging of transistor capacitances to propagate signals, feed-through logic exploits the inherent capacitance of transistor gates to store and transfer charge, thereby minimizing dynamic power dissipation.

The basic principle of feed-through logic involves cascading transistors in a way that allows charge to flow through the gate capacitances, effectively reducing the number of switching transitions and energy consumption. By leveraging this charge-sharing mechanism, feed-through logic circuits can achieve significant power savings compared to traditional CMOS designs, particularly in applications with predominantly static or semi-static signal patterns.

Feed-through logic circuits can be implemented using various transistor configurations, including complementary pass-transistor logic (CPL), pseudo-NMOS logic, and differential pass-transistor logic (DPL). Each configuration offers unique advantages in terms of performance, area efficiency, and power consumption, making feed-through logic a versatile and adaptable design choice for low power applications [5].

2.3. Previous approaches and limitations:

Previous research in feed-through logic has explored various design methodologies and optimization techniques to improve power efficiency and performance. Early approaches focused on basic gate-level designs and empirical optimizations to minimize power

consumption without compromising speed or area efficiency. However, these approaches often suffered from limited scalability and compatibility with complex circuit architectures.

One common limitation of early feed-through logic designs was their sensitivity to process variations and environmental conditions, which could degrade performance and reliability under certain operating conditions. Additionally, the lack of standardized design methodologies and characterization techniques hindered the widespread adoption of feed-through logic in industrial applications.

Furthermore, previous approaches to feed-through logic design may have overlooked critical aspects such as signal integrity, noise immunity, and robustness to process variations, leading to suboptimal performance in practical scenarios. As a result, there is a need for more comprehensive studies evaluating the effectiveness of feed-through logic in diverse application domains and addressing the inherent limitations of existing designs.

2.4. Recent advancements in low power design:

Recent advancements in low power circuit design have fueled renewed interest in feed-through logic as a viable solution for energy-efficient computing. Researchers have proposed novel circuit topologies, optimization algorithms, and design automation techniques to overcome previous limitations and exploit the full potential of feed-through logic.

One notable advancement is the development of hybrid logic families that combine the benefits of feed-through logic with other low power design techniques such as adiabatic logic, reversible logic, and quantum-dot cellular automata (QCA). These hybrid approaches aim to leverage the strengths of each logic family while mitigating their respective weaknesses, resulting in more robust and adaptable designs [6].

Furthermore, advances in process technology, circuit simulation, and characterization methodologies have facilitated more accurate modeling and analysis of feed-through logic circuits, enabling researchers to optimize performance and power consumption at a finer granularity. Techniques such as statistical static timing analysis (SSTA) and process variation- aware design have become essential tools for assessing the impact of process variations on feed-through logic circuits and mitigating their effects through design-level optimizations.

Overall, recent advancements in low power circuit design have paved the way for more efficient and reliable implementations of feed-through logic in real-world applications. By

leveraging these advancements and addressing remaining challenges, researchers can unlock new opportunities for energy-efficient computing and contribute to the development of sustainable electronic systems for the future.

3. Fundamentals of feed through logic:

3.1. Basic principles and operation:

Feed-through logic represents a paradigm shift in the realm of digital circuit design, offering a compelling alternative to traditional CMOS logic by exploiting the inherent capacitance of transistor gates. At its core, feed-through logic operates on the principle of charge sharing, wherein charge stored in the gate capacitance of one transistor is transferred to another transistor's gate capacitance to propagate signals.

The basic operation of feed-through logic can be understood through its implementation in simple gate structures such as NAND and NOR gates. In a feed-through NAND gate, for instance, the input signals control the charging and discharging of the gate capacitances of two transistors connected in series.

This charge-sharing mechanism distinguishes feed-through logic from traditional CMOS logic, where signal propagation relies on direct transistor switching. By minimizing the number of switching transitions and leveraging the capacitive coupling between transistors, feed-through logic achieves significant reductions in power consumption while maintaining signal integrity and speed.

3.2. Advantages and challenges:

The adoption of feed-through logic offers several compelling advantages for low power circuit design. One of the primary advantages is its inherent energy efficiency, stemming from the reduction in dynamic power dissipation achieved through charge sharing. By minimizing the charging and discharging of transistor gates, feed-through logic circuits can achieve substantial power savings compared to conventional CMOS designs, particularly in applications with predominantly static or semi-static signal patterns [5-6].

Additionally, feed-through logic exhibits robustness to process variations and environmental conditions, thanks to its reliance on capacitive coupling rather than direct current flow. This inherent resilience enhances the reliability and yield of feed-through logic circuits, making them well-suited for deployment in harsh or uncertain operating environments.

3.3. Comparison with conventional logic families:

In comparison to conventional logic families such as CMOS, TTL (Transistor-Transistor Logic), and ECL (Emitter-Coupled Logic), feed-through logic offers distinct advantages in terms of power efficiency and performance. While CMOS logic remains the dominant choice for many digital applications due to its versatility and robustness, feed-through logic excels in scenarios where power consumption is a primary concern.

Unlike TTL and ECL, which rely on transistor switching to propagate signals, feed-through logic leverages charge sharing to minimize dynamic power dissipation, making it inherently more energy-efficient. Additionally, feed-through logic exhibits lower sensitivity to noise and process variations compared to TTL and ECL, enhancing its reliability and robustness in practical applications.

4. Improved feed through logic design:

4.1. Design methodology:

The design methodology for improved feed-through logic encompasses a systematic approach to achieve optimal performance, power efficiency, and reliability. This methodology involves several key steps:

Requirement Analysis: Begin by clearly defining the functional requirements, performance targets, and power constraints of the target application. Identify the critical parameters that will influence the design decisions, such as speed, area, and power consumption.

Architecture Exploration: Explore various feed-through logic architectures and topologies to identify the most suitable configuration for the given application. Consider factors such as gate count, fan-out capability, and signal propagation delay in evaluating different architectures.

Transistor Sizing and Configuration: Optimize transistor sizes and configurations to minimize power consumption while meeting performance requirements. Balance the trade-offs between transistor sizing, gate capacitance, and switching speed to achieve the desired performance- power trade-off [7].

Gate-Level Optimization: Implement gate-level optimizations such as logic restructuring, gate merging, and gate sharing to reduce the overall gate count and improve circuit efficiency. Leverage advanced synthesis and optimization tools to automate this process and

explore design alternatives efficiently.

Layout and Routing: Pay careful attention to layout and routing considerations to minimize parasitic capacitance, resistance, and inductance. Adopt layout techniques such as gate clustering, clock tree synthesis, and routing optimization to improve signal integrity and reduce power consumption.

4.2. Circuit architecture:

The circuit architecture of improved feed-through logic is characterized by its efficient utilization of transistor capacitances to minimize power consumption and enhance signal propagation. Several key architectural features contribute to the effectiveness of feed-through logic:

Charge-Sharing Pathways: Design the circuit architecture to facilitate efficient charge-sharing pathways between transistors, enabling smooth signal propagation and minimizing dynamic power dissipation. Implement cascaded transistor configurations to optimize charge transfer and reduce signal delay.

Feedback Loops: Incorporate feedback loops and latch-based structures to enhance circuit robustness and stability. Feedback mechanisms can help mitigate the effects of noise, process variations, and environmental disturbances, ensuring reliable operation under diverse operating conditions [8].

Differential Signal Processing: Exploit differential signaling techniques to improve noise immunity and enhance signal integrity. Differential feed-through logic architectures can effectively suppress common-mode noise and reduce sensitivity to external interference, making them suitable for high-reliability applications.

4.3. Circuit optimization techniques:

To further enhance the performance and power efficiency of feed-through logic circuits, various optimization techniques can be employed:

Gate-Level Optimization: Apply gate-level optimizations such as logic restructuring, gate merging, and gate sharing to reduce the overall gate count and improve circuit efficiency. By minimizing redundant logic and optimizing gate placement, gate-level optimizations help reduce power consumption and improve signal propagation.

Transistor Sizing and Biasing: Optimize transistor sizes and biasing conditions to achieve the desired performance-power trade-off. By adjusting transistor widths, lengths, and bias

voltages, designers can balance speed, area, and power consumption according to the specific requirements of the target application.

Power Gating and Voltage Scaling: Implement power gating and voltage scaling techniques to dynamically adjust power supply voltages and disable unused circuit blocks. By selectively reducing voltage levels and shutting down idle components, power gating and voltage scaling help minimize static and dynamic power dissipation.

Clock Gating and Frequency Scaling: Integrate clock gating and frequency scaling mechanisms to dynamically adjust clock frequencies and enable/disable clock signals based on workload requirements. By reducing clock frequencies during low activity periods and activating clock signals only when necessary, clock gating and frequency scaling help reduce switching activity and power consumption.

4.4. Power reduction mechanisms:

Power reduction mechanisms play a critical role in improving the energy efficiency of feed-through logic circuits. Several key mechanisms can be employed to reduce power consumption:

Dynamic Voltage and Frequency Scaling (DVFS): Implement DVFS techniques to dynamically adjust the supply voltage and clock frequency based on workload requirements. By reducing voltage and frequency during low activity periods and increasing them during peak demand, DVFS helps minimize power consumption without sacrificing performance.

Adaptive Power Gating: Employ adaptive power gating techniques to selectively power down unused circuit blocks or modules during idle periods. By shutting off power to inactive components, adaptive power gating reduces static power dissipation and extends battery life in portable devices [9].

Subthreshold Operation: Explore subthreshold operation modes to achieve ultra-low power consumption by operating transistors in the subthreshold region. Subthreshold operation allows transistors to function at lower voltages and currents, significantly reducing dynamic and leakage power dissipation.

Clock Gating and Dynamic Clocking: Integrate clock gating and dynamic clocking mechanisms to disable clock signals to inactive circuit blocks or modules. By gating the clock signals and reducing clock frequencies during low activity periods, clock gating and dynamic clocking help minimize power consumption without sacrificing performance.

5. Case studies and applications:

5.1. Application scenarios for improved feed through logic:

Improved feed-through logic has found diverse application scenarios across various domains, owing to its exceptional power efficiency and robustness. Some notable application scenarios include:

IoT Devices: In the realm of Internet of Things (IoT), where energy efficiency is paramount due to limited battery life, feed-through logic offers an ideal solution. IoT sensor nodes, wearable devices, and smart home appliances can benefit from the low power consumption and reliability of feed-through logic, enabling prolonged operation and enhanced user experience.

Portable Electronics: Mobile phones, tablets, and other portable electronics rely heavily on battery power, making power efficiency a critical consideration. By incorporating improved feed-through logic, manufacturers can extend battery life, reduce heat dissipation, and enhance the overall user experience by delivering more energy-efficient devices with longer operating times.

Medical Implants: Medical implants such as pacemakers, insulin pumps, and neurostimulators require ultra-low power consumption and high reliability to ensure patient safety and longevity. Improved feed-through logic offers a viable solution for designing energy-efficient implantable devices that can operate reliably for extended periods without the need for frequent battery replacement or recharging.

Aerospace and Defense Systems: Aerospace and defense applications demand ruggedness, reliability, and energy efficiency in harsh operating environments. Improved feed-through logic can meet these requirements by offering robust circuit architectures, low power consumption, and resistance to radiation and environmental hazards, making it suitable for applications such as avionics, navigation systems, and satellite communications.

5.2. Case studies demonstrating power efficiency:

Several case studies have demonstrated the power efficiency and effectiveness of improved feed-through logic in real-world applications. Some notable examples include:

Energy-Efficient Sensor Nodes: Researchers have developed low-power sensor nodes for wireless sensor networks using improved feed-through logic. These sensor nodes exhibit

significantly reduced power consumption compared to conventional designs, enabling long-term operation powered by energy harvesting or small batteries.

Wearable Health Monitoring Devices: Wearable health monitoring devices equipped with improved feed-through logic have been shown to provide continuous monitoring of vital signs such as heart rate, blood pressure, and oxygen saturation with minimal power consumption. This enables users to track their health status conveniently and reliably without frequent battery recharges.

Battery-Powered Embedded Systems: Embedded systems deployed in remote or resource-constrained environments benefit from the energy efficiency of improved feed-through logic. By minimizing power consumption during both active and idle states, these systems can operate autonomously for extended periods on battery power, reducing the need for frequent maintenance and battery replacements.

Spacecraft Onboard Systems: Spacecraft onboard systems require low power consumption and high reliability to ensure mission success in the harsh conditions of space. Improved feed- through logic has been successfully employed in spacecraft onboard computers, communication systems, and scientific instruments, demonstrating exceptional power efficiency and robustness in space missions.

5.3. Practical implementation considerations:

While improved feed-through logic offers compelling advantages in terms of power efficiency and performance, several practical implementation considerations must be addressed:

Technology Compatibility: Ensure compatibility with existing semiconductor manufacturing processes and design tools to facilitate the adoption of improved feed-through logic in industry- standard design flows. Compatibility with standard cell libraries, design rules, and verification methodologies is essential for seamless integration into existing design environments.

Design Tools and Methodologies: Develop specialized design tools and methodologies tailored to the unique characteristics of feed-through logic circuits, such as charge sharing, feedback mechanisms, and differential signaling. These tools should support accurate modeling, simulation, and optimization of feed-through logic designs to achieve optimal performance and power efficiency.

Reliability and Robustness: Address reliability and robustness concerns related to process

variations, aging effects, and environmental conditions to ensure the long-term reliability of feed-through logic circuits in practical applications. Implement design techniques such as redundancy, error correction, and fault tolerance to enhance circuit robustness and mitigate the effects of potential failure mechanisms.

System Integration: Consider system-level integration challenges such as interfacing with external components, signal conditioning, and power management in the design of feed-through logic-based systems. Collaborate with system architects, hardware designers, and software developers to ensure seamless integration and interoperability with other system components.

6. Conclusion:

The review of low power circuit techniques leveraging improved feed-through logic underscores the significant advancements and potential of this innovative approach in addressing the pressing need for energy-efficient electronic systems. Throughout this review, we have explored the fundamental principles, advantages, challenges, design methodologies, case studies, and practical implementation considerations associated with feed-through logic. Improved feed-through logic represents a paradigm shift in digital circuit design, offering a compelling alternative to traditional CMOS logic by leveraging the inherent capacitance of transistor gates to minimize power consumption while maintaining performance. By enabling charge sharing and propagation without direct current flow, feed-through logic achieves substantial reductions in dynamic power dissipation, making it well-suited for applications requiring energy efficiency and reliability. The review has highlighted the diverse application scenarios where improved feed-through logic can make a significant impact, ranging from IoT devices and wearable electronics to medical implants and aerospace systems. Case studies have demonstrated the power efficiency and effectiveness of feed-through logic in real-world applications, showcasing its potential to extend battery life, enhance reliability, and enable new functionalities.

In conclusion, low power circuit techniques leveraging improved feed-through logic hold great promise for enabling the development of energy-efficient, reliable, and sustainable electronic systems to meet the demands of today's increasingly connected and power-constrained world. By harnessing the principles of feed-through logic and addressing practical implementation challenges, researchers and engineers can pave the way for a new era of energy-efficient computing and electronics. Through ongoing innovation and collaboration, feed-through logic has the potential to revolutionize the way we design, build,

and use electronic systems, leading to a greener and more efficient future.

7. References:

(1) Alam, M. A., Mahapatra, S., & Roy, K. (2019). A review of emerging non-volatile memory (NVM) technologies and applications. IEEE Access, 7, 17915-17946.

(2) Choi, S. W., Park, S., Min, K. W., & Kim, C. (2018). A low power high-speed feed-through logic circuit with low process and temperature sensitivity. In 2018 21st International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) (pp. 1-6). IEEE.

(3) Elmasry, M. I., & Williams, D. A. (1996). Low-power VLSI circuits and systems. In Proceedings of the IEEE (Vol. 84, No. 4, pp. 611-632). IEEE.

(4) Liu, Y., Li, Y., Song, K., & Cheng, Y. (2019). A 0.7V 5MHz 0.4nW/100KHz sub-threshold feed-through logic with improved dynamic power consumption. In 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS) (pp. 1025-1028). IEEE.

(5) Najafi, H., & Emadi, S. (2018). High-speed low-power feed-through logic using 45nm technology. Journal of Circuits, Systems and Computers, 27(08), 1850139.

(6) Roy, K., & Mukhopadhyay, S. (2009). Low power CMOS VLSI circuit design. John Wiley & Sons.

(7) Sukhwani, B., & Joshi, R. M. (2017). A review on design and analysis of low power CMOS circuits. In 2017 International Conference on Innovations in Electrical, Electronics, Instrumentation and Media Technology (ICEEIMT) (pp. 296-300). IEEE.

(8) Weste, N. H. E., & Harris, D. (2010). CMOS VLSI design: A circuits and systems perspective. Addison- Wesley.

(9) Chouhan, S., & Sharma, A. (2015, March). Performance analysis of STBC coded MIMO-OFDM system for WIMAX (IEEE 802.16) systems. In 2015 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS) (pp. 1-6). IEEE.