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Low power multiplexer design using CMOS device modeling

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Abstract:

Low power and high speed digital circuits are basic needs for any of digital circuit; De-multiplexer is a basic circuit for any digital circuit. In this paper de-multiplexer has been designed using CMOS, transmission gate pseudo nmos logic. The performance of designs has been compared in terms of power consumption, delay and transistor counts. The proposed design demonstrates the superiority in terms of power dissipation, delay and transistor counts, compared with existing 1:4 de-multiplexer and comparative analysis on 90nm and 45nm technology. The schematic of developed de-multiplexer has been designed and simulated using Tanner EDA tool.

Keywords:

Moore's law, Universal gates, CMOS technology.