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Low power multiplexer design using CMOS device modeling

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Abstract:

Low power and high speed digital circuits are basic needs for any of digital circuit; De-multiplexer is a basic circuit for any digital circuit. In this paper de-multiplexer has been designed using CMOS, transmission gate pseudo nmos logic. The performance of designs has been compared in terms of power consumption, delay and transistor counts. The proposed design demonstrates the superiority in terms of power dissipation, delay and transistor counts, compared with existing 1:4 de-multiplexer and comparative analysis on 90nm and 45nm technology. The schematic of developed de-multiplexer has been designed and simulated using Tanner EDA tool.

Keywords:

Moore's law, Universal gates, CMOS technology.

1. Introduction:

In today's world power consumption is become major power concern in VLSI designing. Portable devices like laptops, cell phones, and computers require a circuitry that consumes less power. Also large power dissipation is directly associated with cost and complexity of the devices. High speed multiplier plays a dominant role in designing of digital circuits. The low power CMOS devices can be used in real time image, speech processing and 3D computers graphics application, mainly the fields where high speed is required.

In CMOS logic in CMOS devices the half power is dissipated design in PMOS network and stored energy is dissipated during discharging process of output load capacitor during the switching events. Most of the power consumption reduction techniques are based upon scaling of the supply voltage, reducing capacitance and switching activity. Yet in all these cases, energy drawn from the power supply is used only once before being dissipated. Thus to increase the energy efficiency of logic circuits, a technique is required that can reuse the energy stored on load capacitor. It has been found that there is a fundamental relation between computation and power dissipation. That is if somehow computation could be implemented without any loss of information, then the energy required by it could be potentially reduced to zero. This can be done by performing all computation in reversible manner. Also energy dissipation depends upon average voltage drop traversed by charge that flows on to the load capacitance. By using smaller voltage steps or increments dissipation can be reduced. The minimum power consumption during the charge transfer phase is termed as adiabatic switching. In adiabatic logic charging is done by constant current source instead of constant voltage source as in conventional CMOS logic.

Due to the limited power supplied by the batteries, the circuitry involved in these devices must be designed to consume less power. Also large power dissipation requires expensive and noise cooling machinery, batteries and power conservation circuits. Multiplexer is essential component in digital design. It is extensively used within data path-intensive designs. Thus minimizing the power dissipation of the multiplexer is one of the main concerns of low power design. Most of the power saving techniques involved scaling of the power supply, which results, substantial increase in sub-threshold leakage current also it causes uncertainty in the process variation

2. Proposed techniques to solve problems:

2.1 Conventional CMOS technique:

In conventional or complementary CMOS logic gates are made up of a PMOS pull-up and a NMOS pull down logic network. CMOS logic style has an advantage of robustness against voltage scaling and transistor sizing. It has high noise margins and operates reliably at low voltages. Connection of input signals to transistor gates only, facilitates the usage and characterization of logic cells. The complementary transistor pair makes the layout of CMOS gates efficient and straightforward. The major disadvantage of CMOS is substantial number of large PMOS transistors which results in high input loads. In this logic style, both N-type and P-type transistors are used to realize logic functions. The same signal which turns on a transistor of one type is used to turn off a transistor of the other type. This allows the design of logic devices using only simple switches, without the need for a pull-up resistor. In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull down network between the output and the lower voltage power supply rail and the collection of p-type MOSFETs in a pull up network between the output and the higher voltage rail. Thus, if both p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be on when the n-type MOSFET is off, and vice-versa. A 2to1 multiplexer can be implemented using 8 transistors by this logic style. Fig. 1 shows 2 to1 multiplexer Using CMOS logic style.

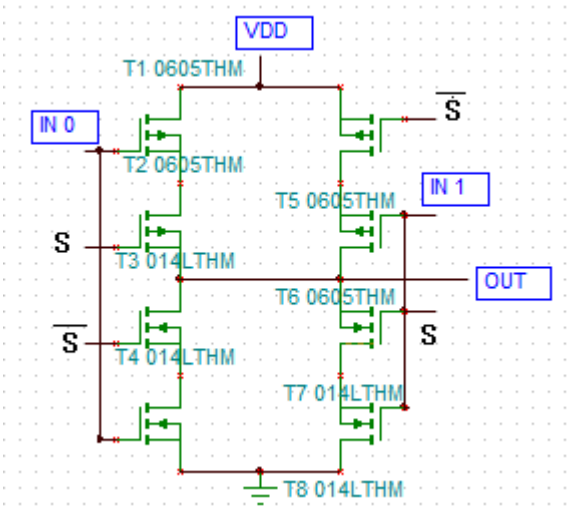


Figure. 1 2to1 inverted multiplexer using CMOS

In this subsection the complementary CMOS style is presented as a kind of MUX structure with its own properties. It is the static style which has the combination of PMOS transistors as Pull-Up Network (PUN) and NMOS transistors as Pull down Network (PDN). The PUN connects the VDD to output and the PDN makes the connection between VSS and output. The two networks function in a mutually exclusive fashion. Only one network is conducting in

steady state. Hence the output is connected to VDD or VSS depends on the input pattern. Compare to the other methods, this style is a robust design with full swing at its output. It is also a reliable design because of the static approach. It exhibits a rail-to- rail swing with VOH = VDD and VOL= GND. There is no static power consumption due to the mutually exclusive PDN and PUN.

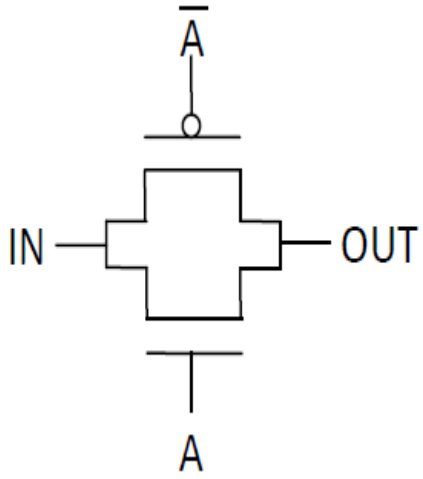
To analyze the circuit efficiently, it is important to apply the input patterns such that they will cover all possible combinations and their output. Generally, the static style has more current flow than that of pass transistor logic (CPL). Hence it has lower gate delay and the circuit propagates faster than that of the CPL. The gate delay as mentioned in can be calculated as

$$tpd \propto CLVdd/IDS$$

Where, TDP is the propagation delay, *CL* is the load Capacitance, VDD is the supply voltage and *IDS* is the drain saturation current. The other advantages of this method are no charge sharing problem and glitch free. Whereas the dynamic style and pass transistor methods are affected by these factors. Hence from we can understand that the drawback of the static MUX structure when compared to Pass transistor style is the higher power usage.

2.2 Transmission gate (TG) logic style:

This section describes the purpose and basic operation of a transmission gate. The transmission gate can be used to quickly isolate multiple signals with a minimal investment in board area and with a negligible degradation in the characteristics of those critical signals. A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. The solid-state-switch is comprised of parallel connection of a PMOS transistor and NMOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off. When the voltage on node A is a Logic 1, the complementary Logic 0 is applied to node active-low A, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node active-low A is a Logic 0, the complementary Logic 1 is applied to node A, turning both transistors off and forcing a high-impedance condition on both the IN and OUT nodes. This design provides true bidirectional connectivity without degradation of the input signal.



A	IN	OUT
H	H	H
H	L	L
L	X(don`t care)	Z(high impedance)

Figure. 2: Transmission gate: graphical symbol, truth table

In this logic style N and P devices with sources and drains connected in parallel. Vg is the control signal for the N device, Vgc (complement of Vg) is the control signal for the P device. So When Vg is high (at Vdd) and Vgc is therefore low (at Gnd), the NFET and PFET are both ON. (Depending upon the devices' source potentials, one may be ON more strongly than the other.) The switch is therefore CLOSED and VOUT will be the same logic level as VIN. When Vg is low (at GND) and VGC is high (at VDD), both devices are OFF. The switch is therefore OPEN and VOUT will be independent of VIN. A 2 to1 multiplexer can be implemented using 6 transistors by this logic style. Fig.3 shows 2to1 multiplexer using transmission gate logic style.

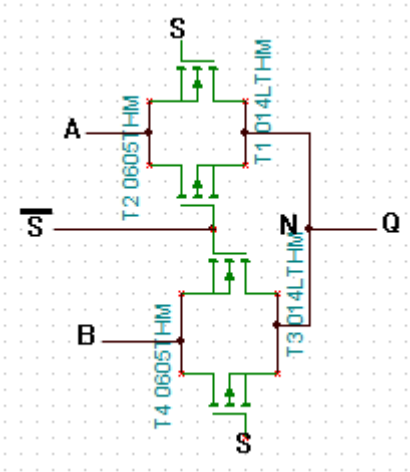


Figure. 3: 2to1 multiplexer using Transmission Gate

This is the Transmission Gate type of MUX structure implemented with very minimum transistors (4 MOS transistors) compared to the complementary static method which has 10

CMOS devices. The back to back connected PMOS and NMOS arrangement which acts as a switch is called Transmission Gate. NMOS devices pass a strong 0, but a weak 1, while PMOS devices pass a strong 1, but a weak 0. The Complementary Static CMOS uses NMOS as pull down and PMOS as pull up, whereas transmission gate combines the best of both the properties by placing NMOS in parallel with the PMOS device. Two transmission gates are connected as in figure 4 to form a MUX structure. The TGL method has very few nodes to compute a function. Due to this reason, the energy requirement is very low. Each Transmission Gate acts as an AND switch to replace the AND logic gate which is used in a conventional gate design of MUX. Hence the device count is reduced to 4. One more change when compared to static method is that there is no supply voltage applied to the circuit. It is also another reason for low operating power. But the delay is more than the static style which is clear from. This is due to the weak driving capability of the circuit. The electric field strength is low because of the absence of VDD.

3. Result:

3.1. Schematic of MTCMOS 2:1 MUX Cell:

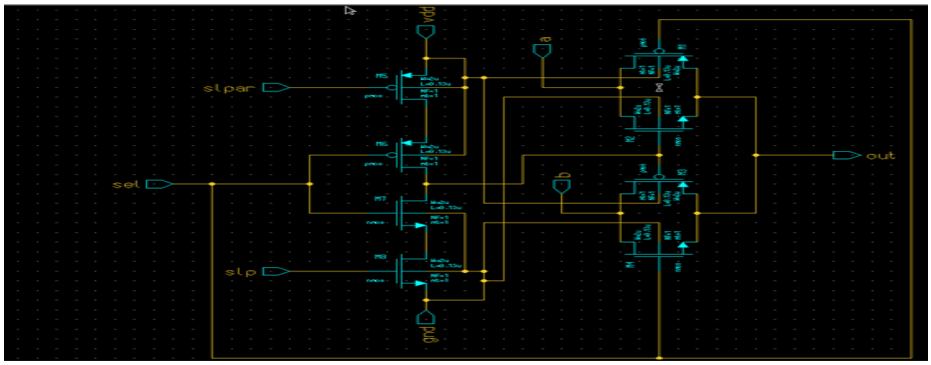


Figure. 4:

In the schematic diagram of MTCMOS 2:1 mux we design the mux by using the mtcmos technique where, the two sleep transistor is uesd to prevent from the leakage power because they have the characteristics to suppress the leakage power and the CMOS invertor is used as to provide the select line which has the low threshold voltage. So when the select line is high then it gives the output which is equal to the input A. when the select line is low then it gives the result which is equal to the input B. we use 45 nm technology to find the result, so we take the input voltage which is 1.8 v and vary the threshold voltage from .9 to 1.4 volt. So 2:1 mux consume least power by using the MTCMOS technique as compare to the other techniques.

3.2. Test circuit of 2*1 MTCMOS MUX:

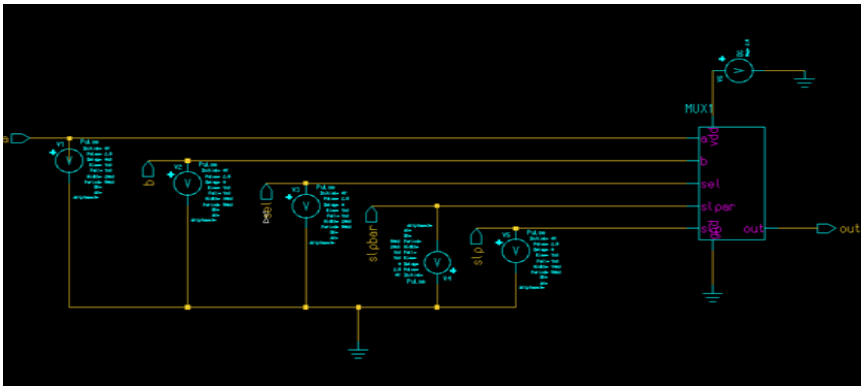


Figure. 5:

This is the test circuit of the MTCMOS MUX in this we take the IC of the MTCMOS MUX in this we discuss about the connection of the circuit. We use two input and one select line and two sleep transistors which has high threshold voltage. CMOS invertor is used as a select line.

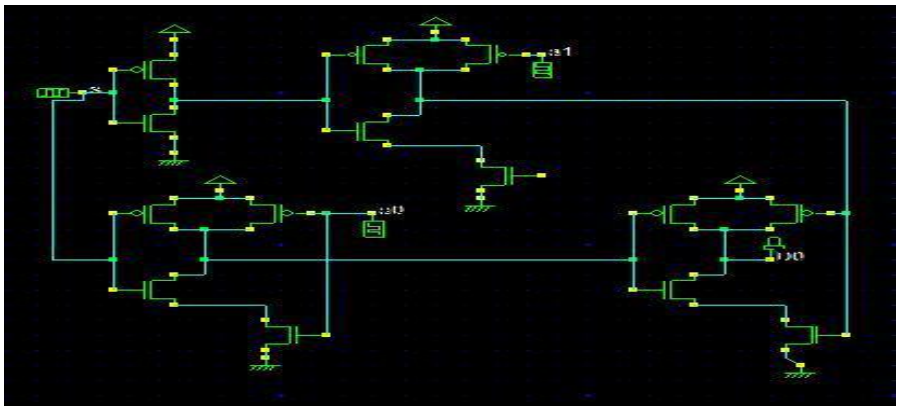


Figure. 6:

Here we use the transmission gate technique to design the multiplexer.

3.3. Mux PTL XOR/XNOR:

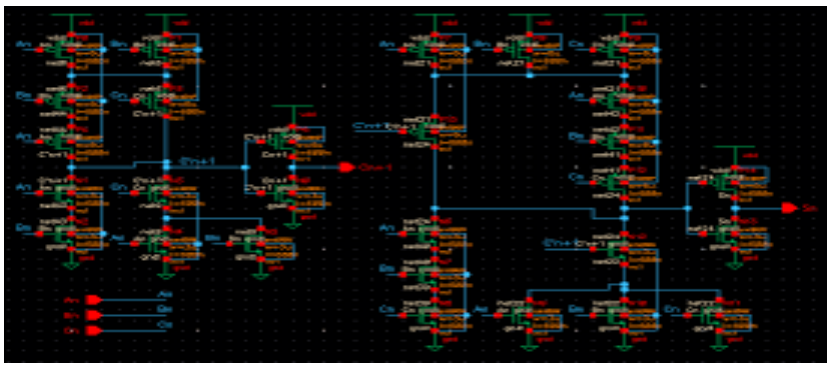


Figure. 7:

We design mux by using the pass transistor logic so in which first implement the XOR or XNOR.

3.4. Basic MUX using CMOS:

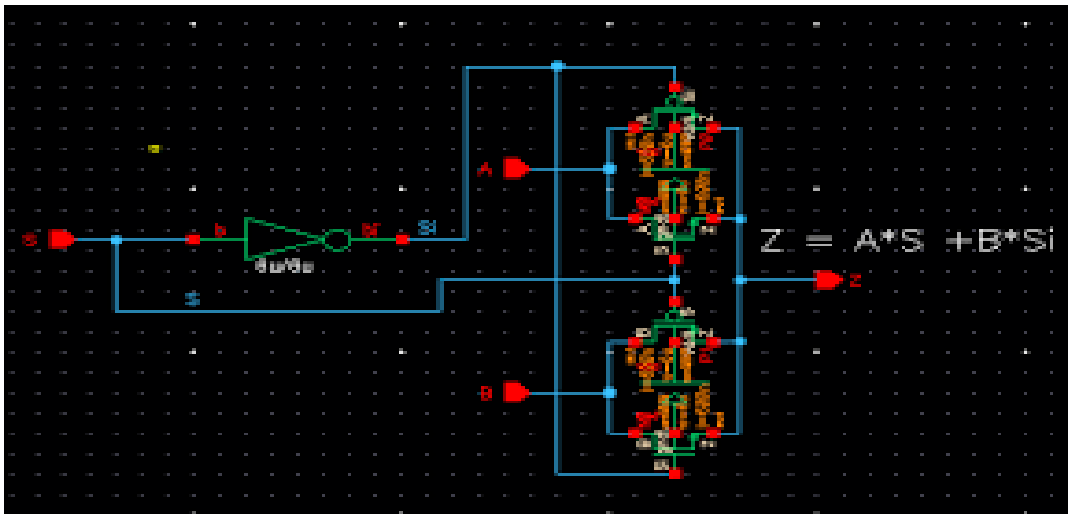


Figure. 8:

To design the multiplexer by using CMOS technique then we take an inverter which is act as a select line. To design 2:1mux using two input A and input B. So when select line is high then it only selects input as an output. And when the select line is low hen it only selects input B as an output.

3.5. Output of MUX variable input:

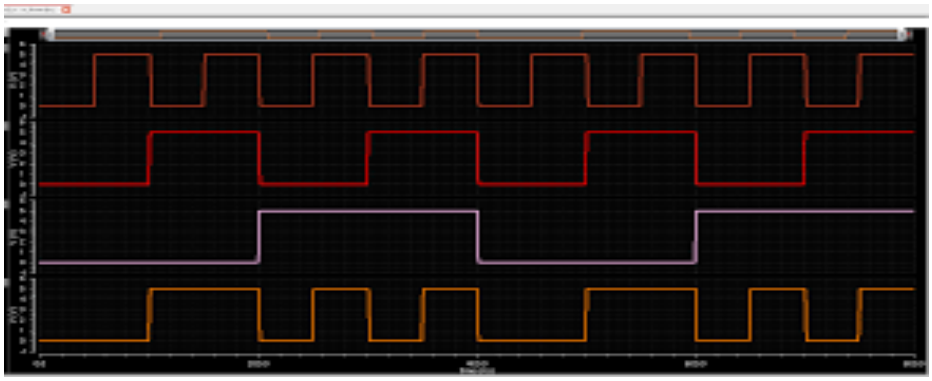


Figure. 9:

Here first and second waveform is the input and light violet waveform is select line and yellow waveform is output. So when the select line is high then it only be select input A as an output and when the select line is low then it only be select input B as an output.

3.6. Output graph for leakage power:

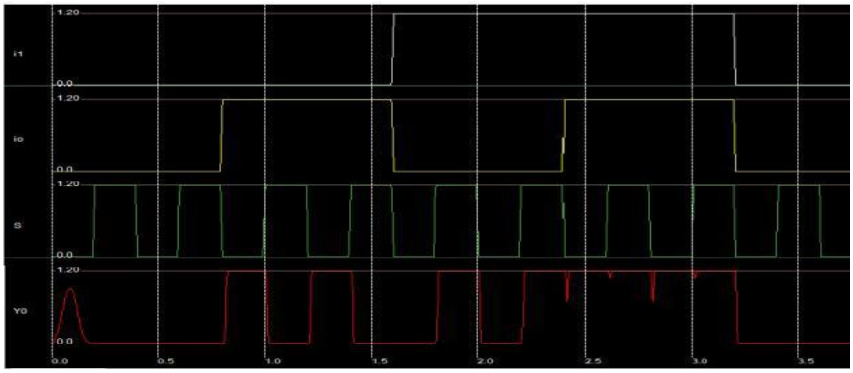


Figure. 10:

It is graph for the leakage power in output we check the leakage in a very small amount of time in the output. The red waveform is the output waveform and peak wave indicate the leakage in output.

3.7. 4*1 MUX CELL:

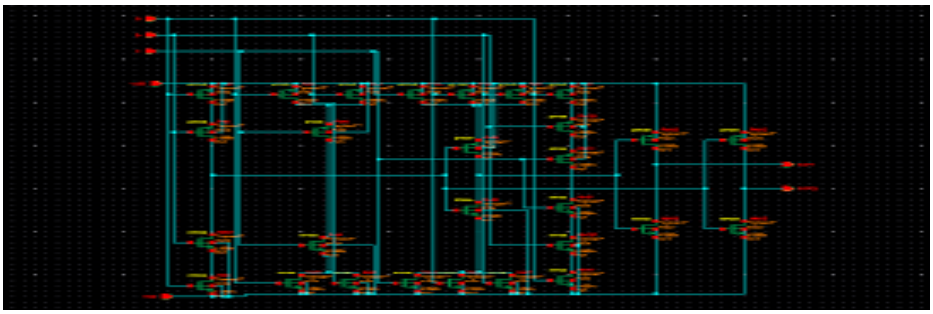


Figure. 11:

It is the multiplexer cell for 2:1 mux. So we use four input and two select line which give only one output.

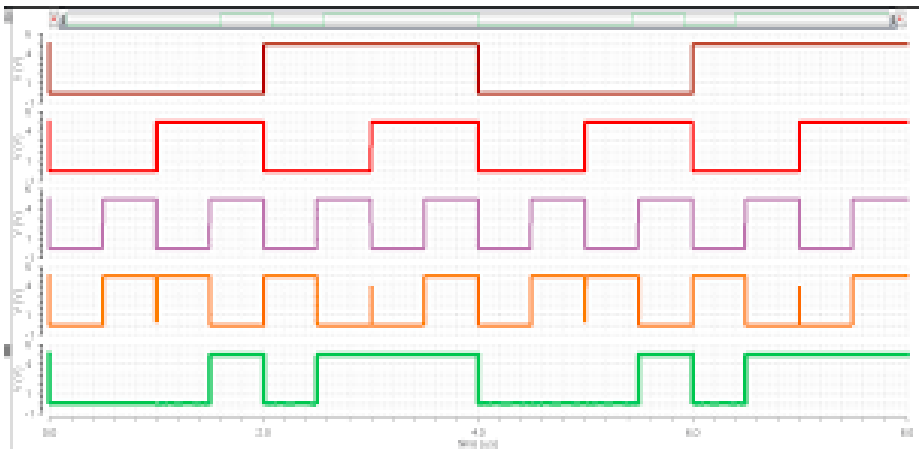


Figure. 12:

3.8. Output waveforms of mux using CMOS:

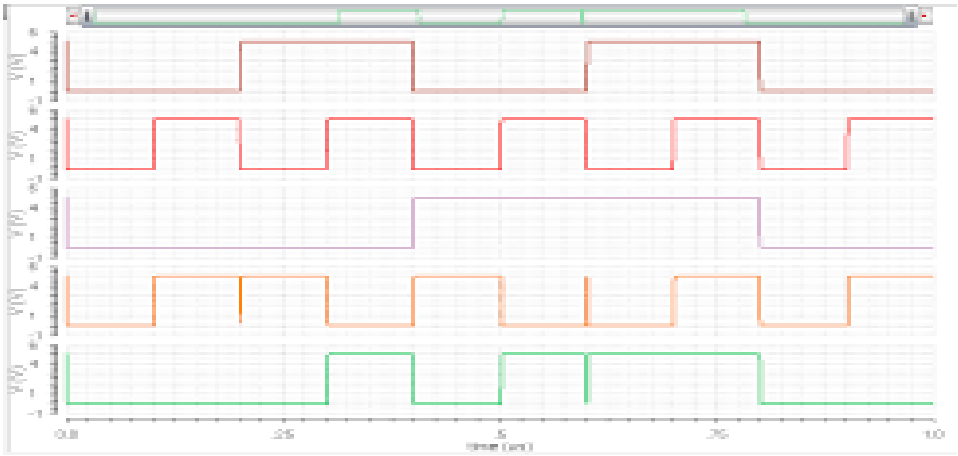


Figure. 13:

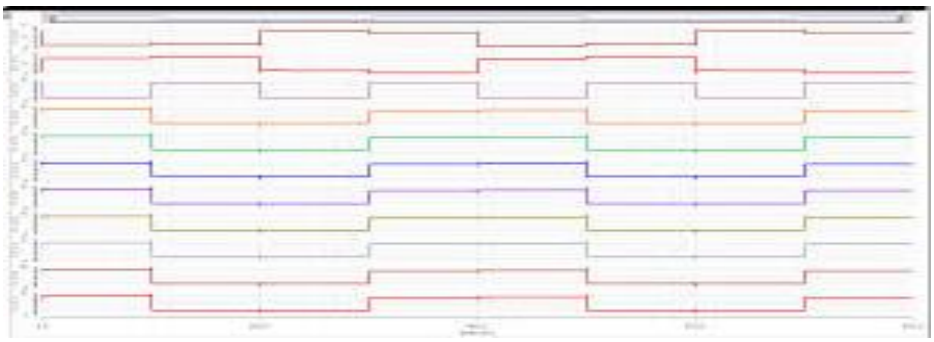


Figure. 14:

4. Comparison of results using different techniques:

4.1. Comparison of transistors:

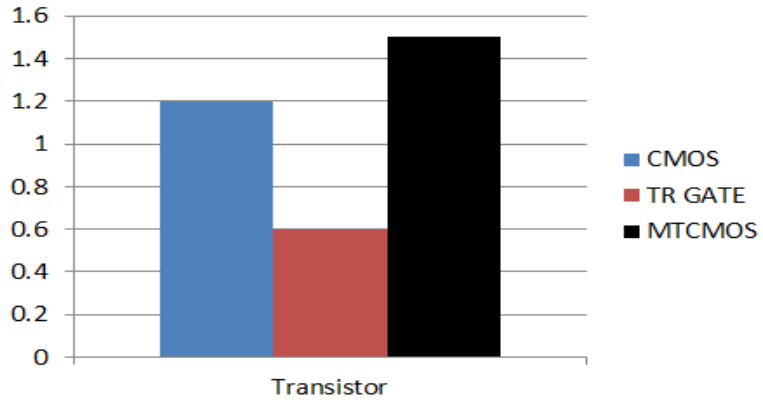


Figure. 15:

Here we compare of between three different techniques which is CMOS, MTCMOS and Transmission gate. In transmission gate technique which uses least number of transistors. In MTCMOS technique number of transistors increases by using sleep transistors.

4.2. Comparison of area:

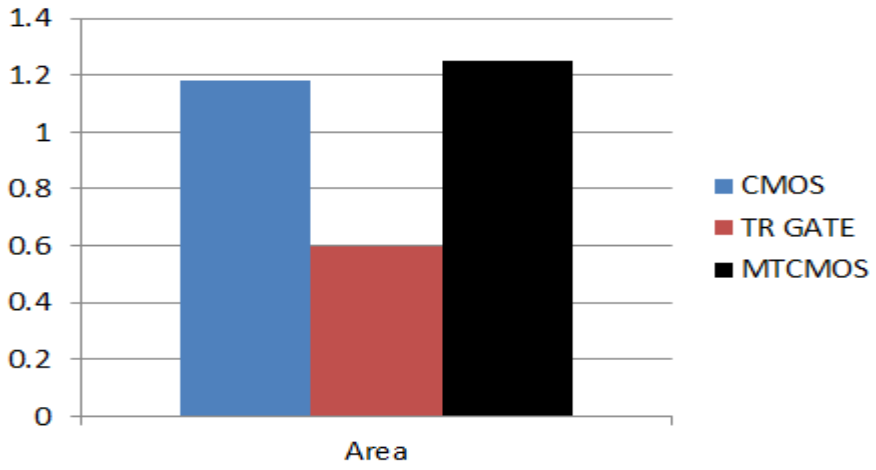


Figure. 16:

The area of MTCMOS mux increases because of the sleep transistors. The area of TR Gate is least because in this technique it eliminating the redundant transistors.

4.3. Comparison of power:

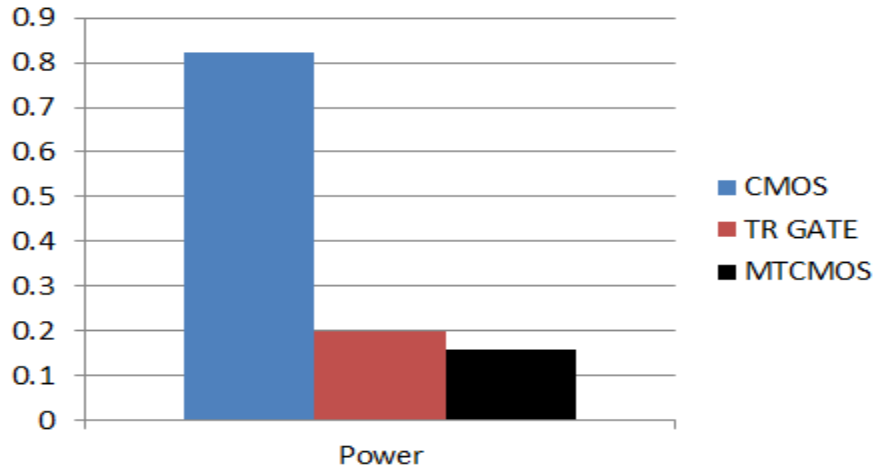


Figure. 17:

In the MTCMOS technique it consumes least amount of power as compare to the other techniques. The power consumption is decreases then the power dissipation will also decrease.

4.4. Comparison of deay:

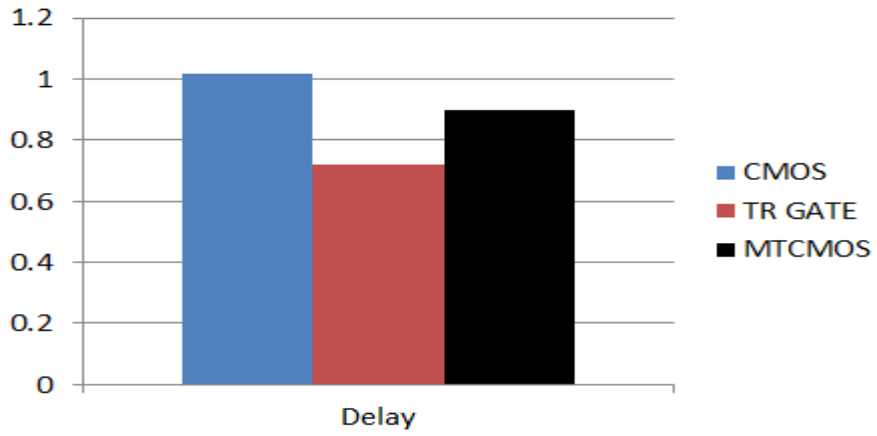


Figure. 18:

The CMOS technique has high delay as compare to the other techniques. But the transmission gate technique has low delay and in MTCMOS technique it has delay but it is least as compare to the CMOS techniques.

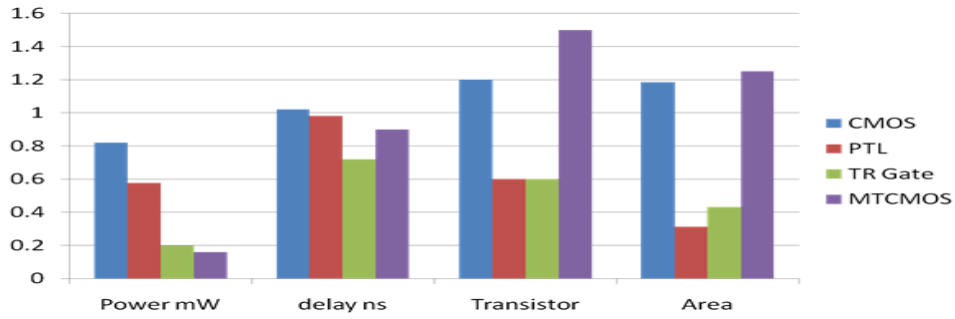


Figure. 19:

5. Conclusion:

Multiplexer can work on analog as well as digital data. Multiplexer are built of relays and transistor switches for analog application but for digital applications, they are built from standard logic gates. The multiplexer is used for digital applications, also called digital multiplexer, is a circuit with many input but only one output. By applying control signals, we can steer any input to the output. Multiplexers and de-multiplexers are common building blocks of data paths and are used extensively in numerous applications including processor buses, network switches and digital signal processing stages incorporating resource sharing. Multiplexer designed for biomedical applications are low power consumption low on resistance and faithful reproduction of input at the output. Multiplexer are used in various fields where multiple data need to be transmitted using a single line. Following are some of the applications of multiplexers –

1. Communication System- Communication Process is the process of transmitting information of the dedicated channel, which is received at the receiver side and such type of system is called communication system. The efficiency of communication system can be increased with the help of multiplexer. Multiplexer is used in the communication system to transmit different type of information, such as audio or video at the same time on a single transmission line.
2. Telephone network - Multiplexer is widely used in the telephone network to multiplex various audio signals on single line. In this way multiple audio signals can reach to the dedicated recipients with the help of multiplexer.
3. Computer memory – Another application of the multiplexer is to implement computer memory. It also reduces the number of copper wire to connect the memory with other computer parts.
4. Transmission from the computer system of a satellite – Multiplexer can be used in the satellite communication. It is used to transmit data from satellite or spacecraft to the ground system with of help of GPS (Global Positioning System).

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